Senior Design 405

Design Capture Requirements

1/22/10

Filipe Betzel

Adam Hoffert

Tom Narvesen

Zachary Skalsky

Introduction:

Our team will create a basic microcontroller using an open source processor core and three custom peripherals. The peripherals will be designed, tested and implemented by our team while learning about design practices, concepts and tools.

Requirements:

- The team will build from scratch three peripherals for an open source processor core using RTL
  The three peripherals will be:
  - UART
  - SMBUS version 1.0 – verified with 3rd party hardware/software
  - LCD Interface - Allows uP to interface to LCD screen on Altera DE2
- Device Requirements
  1. Implement method of using RAM and ROM for microprocessor
  2. Have general input/output ports for controlling external devices
  3. Device will run compiled C code from a compiler designed for reference controller
  4. RTL will run on commercially available FPGA demo board
  5. Design test applications to demonstrate device operability
  6. Demonstrate stable behavior by executing a program the same way as the reference controller would
  7. Learn the layout and extraction tools well enough to perform at least a partial layout
  8. Develop a real world application for device

Final Deliverables:

- Verilog code for all core, peripheral and system components
- Test programs written in C, simulations done in Simvision and Verilog testbenches demonstrating system and component operability
- Synthesized Verilog, Quartus projects and SDC constraints for operating device on an Altera FPGA
- Detailed datasheet on device operation
- Deliver one functional hardware unit

Objectives:

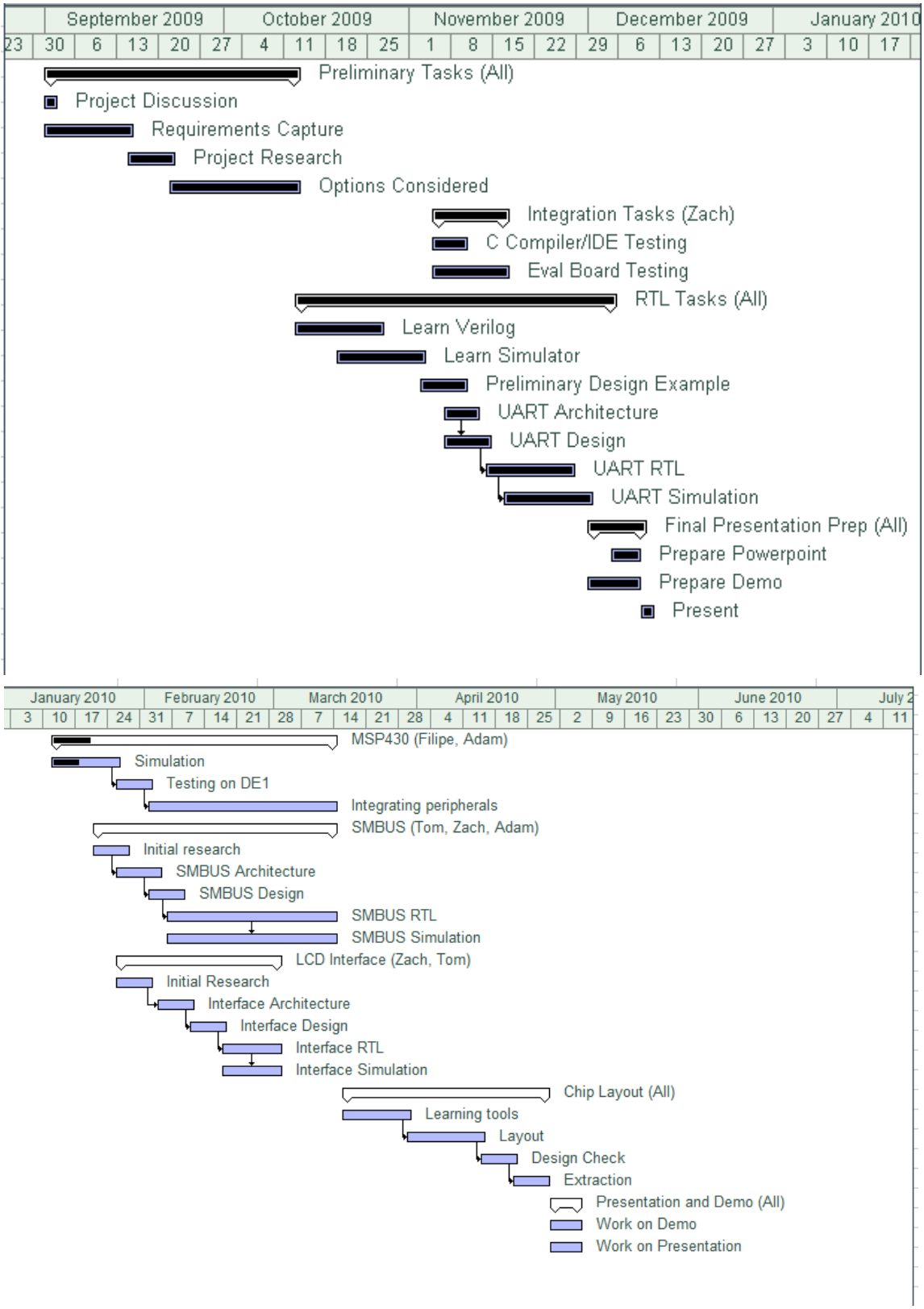
- During this project, the team will work on developing the following skills
  - Developing and simulating RTL code
  - Knowledge of revision control
  - Knowledge of FPGA design and use
  - Understanding of digital communication busses
  - Project management skills
  - Design for test principles

This document describes all project requirements set forth by the advisor and or client. Grading will be performed at the end of the semester according to the level at which these requirements are met.

BUDGET

Parts	Price	Academic Price	QTY	Total
Altera DE1 Board	$150	$125	1	$125
Altera DE2 Board	$495	$269	1	$269
Internal PCB	$0	$0	2	0
Parts estimate	$30	$30	1	$30
Cadence Simvision	$0	$0	4	0
Altera Quartus II	$0	$0	4	0
Mentor Graphics Modelsim	$0	$0	4	0
Texas Instruments IAR Compiler	$0	$0	4	0
Cadence Virtuoso	$0	$0	4	0
Shipping	$10	$10	4	$40
TOTAL				$464

Timeline


September 2009
October 2009
November 2009
December 2009
January 2010
23 30 6 13 20 27 4 11 18 25 1 8 15 22 29 6 13 20 27 3 10 17
Preliminary Tasks (All)
Project Discussion
Requirements Capture
Project Research
Options Considered
Integration Tasks (Zach)
C Compiler/IDE Testing
Eval Board Testing
RTL Tasks (All)
Learn Verilog
Learn Simulator
Preliminary Design Example
UART Architecture
UART Design
UART RTL
UART Simulation
Final Presentation Prep (All)
Prepare Powerpoint
Prepare Demo
Present
January 2010
February 2010
March 2010
April 2010
May 2010
June 2010
July 2
3 10 17 24 31 7 14 21 28 7 14 21 28 4 11 18 25 2 9 16 23 30 6 13 20 27 4 11
MSP430 (Filipe, Adam)
Simulation
Testing on DE1
Integrating peripherals
SMBUS (Tom, Zach, Adam)
Initial research
SMBUS Architecture
SMBUS Design
SMBUS RTL
SMBUS Simulation
LCD Interface (Zach, Tom)
Initial Research
Interface Architecture
Interface Design
Interface RTL
Interface Simulation
Chip Layout (All)
Learning tools
Layout
Design Check
Extraction
Presentation and Demo (All)
Work on Demo
Work on Presentation